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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,061	10/28/2003	Seong-Ho Kim	5649-1168	5437

7590 07/18/2005

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,061	KIM ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,27-35 and 37-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7,30 and 34* is/are allowed.

6)☒ Claim(s) *27-29,31-33,35 and 37-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation "the silicon nitride liner contacts the self-aligned contact pad at the bottom portion of each gate electrode with a thicker covering than other parts thereof' (claim 40) must be shown or the feature(s) canceled from the claim(s). Note that although Figures 1 and 2 show a thicker covering at that portion, the thicker covering consists of two separate liners, not a single liner as claimed. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 40 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "the silicon nitride liner contacts the self-aligned contact pad at the bottom portion of each gate electrode with a thicker covering than other parts thereof" is not supported by the originally filed application. Figures 1 and 2 show a thicker covering at the bottom portion of the self-aligned contact pad, but the thicker covering results from two separate liners overlapping each other, not a single liner as claimed. The specification and drawings do not support "a silicon nitride liner" with a thicker covering at the bottom portion. Therefore, the above limitation constitutes new matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 27-29, 35, and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (US Pat. 6,294,449, hereinafter Wu).

Regarding claim 27, Figure 7 of Wu discloses a plurality of gate electrodes 30 disposed on a substrate 10, the gate electrodes having opposing sidewalls and top and bottom surfaces, wherein portions of selected adjacent sidewalls of neighboring electrodes angle generally downwardly and inwardly toward each other while the opposing sidewall of each of the selected sidewalls are substantially linear, and wherein the angled neighboring sidewall portions have a generally constant downward slope from a top portion of respective gate electrode to about a medial portion thereof, and wherein for a respective selected gate electrode, the opposing sidewall has a different profile shape (i.e., straight). See attached sheet, which further illustrates how Figure 7 of Wu reads on the claimed invention.

Regarding claim 28, Figure 7 of Wu discloses a plurality of elongate contact windows, a respective one positioned between the selected sidewalls of neighboring electrodes 30, wherein the contact window sidewalls comprise an angled profile with an angled portion (see attached sheet) having a generally constant slope that correspond to the angled gate electrode sidewall configuration; and a contact pad 110 disposed in each contact window, the contact pad extending generally downwardly and having a length (height) that is greater than the height of the gate electrode. Note that Wu discloses the device is used in an array (col. 2, lines 3-10); therefore there must be more than one contact.

Regarding claim 29, Figure 7 of Wu discloses a gate protection liner layer 135 that extends in the contact window and covers the angled sidewall portion of a respective gate

electrode; and a first liner layer 55 that covers the remaining surfaces of the top and opposing sidewalls of the respective gate electrode.

Regarding claim 31, Figure 7 of Wu discloses a plurality of gate electrodes 30 disposed on a substrate 10, the gate electrodes having opposing sidewalls and top and bottom surfaces, wherein portions of selected adjacent sidewalls of neighboring electrodes angle generally downwardly and inwardly toward each other while the opposing sidewall of each of the selected sidewalls are substantially linear (see attached sheet); a plurality of elongate contact windows, a respective one positioned between the selected sidewalls of neighboring electrodes 30, wherein the contact window sidewalls comprise an angled profile having a generally constant slope that correspond to the angled gate electrode sidewall configuration (see attached sheet); and a contact pad 110 disposed in each contact window, the contact pad extending generally downwardly and having a length (height) that is greater than the height of the gate electrodes; a gate protection liner layer 135 that extends in the contact window and covers the angled sidewall portion of a respective gate electrode; and a first liner layer 55 that covers the remaining surfaces of the top and opposing sidewalls of the respective gate electrode, wherein the bottom surface of the gate electrodes reside on the semiconductor substrate, and wherein the remaining external surfaces are covered by at least one of the first and second liner layers so that the gate electrodes are encased. Note that Wu discloses the device is used in an array (col. 2, lines 3-10); therefore there must be more than one contact.

Regarding claim 35, Figure 7 of Wu discloses a conductive contact 110 on a substrate 10 in a recess (recess in dielectric layer 60) adjacent to a gate electrode 30 having an opposing top and bottom and a gate electrode sidewall that extends from a top surface to the bottom of the

sidewall, the gate electrode sidewall angling inwardly with a generally constant slope from the top surface to an intermediate portion of the sidewall (middle point of sidewall) toward the recess with a lower portion of the sidewall being substantially vertical so that the bottom of the electrode has a greater width than the top, the conductive contact having a profile with an angled portion having a generally constant slope that corresponds to the slope of the angled gate electrode sidewall and an upper portion that extends above the top surface of the gate electrode. See attached sheet.

Regarding claim 37, Figure 7 of Wu discloses two adjacent gate electrodes 30 on a substrate 10, each gate electrode having a top portion narrower than a bottom portion; a silicon nitride liner 55 covering each gate electrode; and a self-aligned contact pad 110 between the adjacent two gate electrodes, the self-aligned contact pad protruding from a top surface of each gate electrode.

Claims 37-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Sung et al. (US Pat. 6,284,596, hereinafter Sung).

Regarding claim 37, Figure 2I of Sung discloses two adjacent gate electrodes 160 on a substrate 100, each gate electrode having a top portion (adjacent oxide layer 190') narrower than a bottom portion; a silicon nitride liner (part of layer 170) (col. 7, lines 19-22) covering each gate electrode; and a self-aligned contact pad 210 between the adjacent two gate electrodes, the self-aligned contact pad protruding from a top surface of each gate electrode.

Regarding claim 38, Figure 2I of Sung discloses a buffer insulating layer 190' between the silicon nitride liner (part of layer 170) and the self-aligned contact pad 210 at the top portion of each gate electrode.

Regarding claim 39, Figure 2I of Sung disclose the buffer insulating layer 190' comprises a silicon oxide layer (col. 7, lines 45 and 46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Lee et al. (US PGPub 2002/0195672, hereinafter Lee).

Regarding claim 32, Figure 7 of Wu discloses first and second gate electrodes 30 disposed on a semiconductor substrate 10, the first and second gate electrodes having opposing first and second sidewalls and top and bottom surfaces, wherein portions of the adjacent sidewalls of the first and second gate electrodes are configured to angle generally downwardly and inwardly toward each other with a generally constant slope from a top portion to at least about a medial portion thereof (see attached sheet); a contact window positioned between the adjacent sidewalls of the first and second gate electrodes, wherein the contact window sidewalls comprise an angled profile with an angled portion having a generally constant slope that

corresponds to the slope of the angled portion of the gate electrode sidewalls (see attached sheet); and a contact pad 110 disposed in the contact window, the contact pad extending generally downwardly and having a length (height) that is greater than the height of the gate electrode. The difference between Wu and the claimed invention is a peripheral circuit region comprising a gate electrode; lightly doped impurity regions on each side of the gate, and heavily doped impurity regions surrounding the lightly doped regions (i.e., an LDD structure). Figure 3 of Lee discloses a peripheral circuit region b comprising a gate electrode 19 with an LDD structure. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Wu by including a peripheral circuit region including a gate with an LDD structure for the purpose of integrating different types of transistors on the same chip, while reducing short channel effects in the peripheral transistor(s).

Regarding claim 33, Figure 7 of Wu discloses a gate protection liner layer 135 that extends along the sidewalls of the contact window and covers the angled sidewall portion of a respective gate electrode 30 in the cell array region; and a first liner layer 55 that covers target surfaces of the gate electrodes disposed in the cell array region, wherein the adjacent gate electrode angled sidewall portions merge into respective lower substantially vertical portions.

Allowable Subject Matter

Claims 1-7, 30, and 34 are allowed.

The reasons for allowance were provided in the Office Action mailed February 9, 2005.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments filed May 5, 2005 have been fully considered but they are not persuasive.

Applicant argues that Wu does not disclose the newly added limitations. For example, Applicant argues that, "Wu fails to teach or suggest that the angled portion of the sidewall has a generally constant slope from a top surface to an intermediate portion". As explained above, Figure 7 of Wu does disclose all the claimed features. However, as explained in the above rejection (and illustrated in the attached figure), Figure 7 of Wu discloses all limitations of claims 27-29, 35, and 37.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Matthew C. Landau

Examiner

July 12, 2005

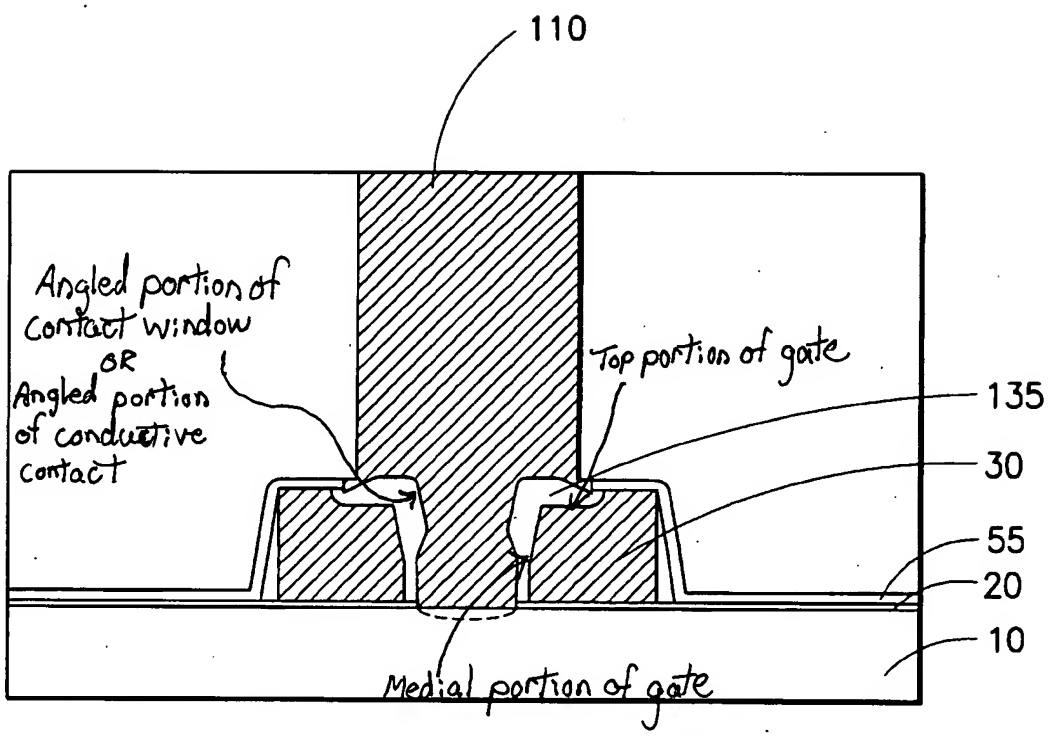
110
Angled portion of contact window
OR
Angled portion of conductive contact
Top portion of gate
135
30
55
20
10
Medial portion of gate

FIG.7